IDEC Chip Design Contest

Stochastic Computing based Machine Learning for Embedded System

Su Yeon Jang*, Chang Yeop Han, Young Hyun Yoon, and Seung Eun Lee
Department of Electronic Engineering,
Seoul National University of Science and Technology

서울과학기술대학교 SEOULTECH SEOUL NATIONAL UNIVERSITY OF SCIENCE & TECHNOLOGY

SoC Platform Lab
SoC 플랫폼 연구실

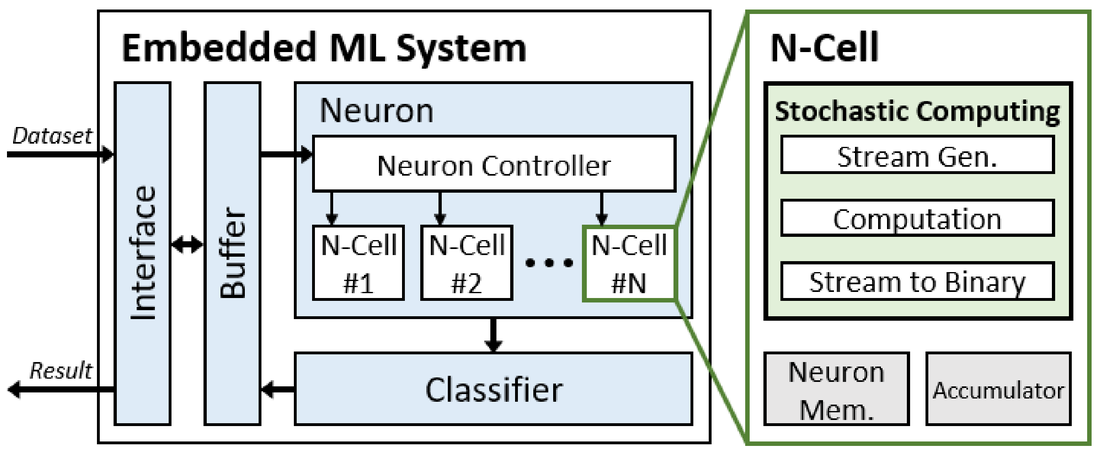
Abstract

Recently, the artificial intelligence (AI) technology is used widely. In order to achieve high accuracy with AI, the AI system needs more complex computing. In the embedded system, however, it has a limitation of resources. The limitation makes hard to implement a complex calculation in embedded systems. In order to overcome the limitation, embedded systems need a dedicated module.

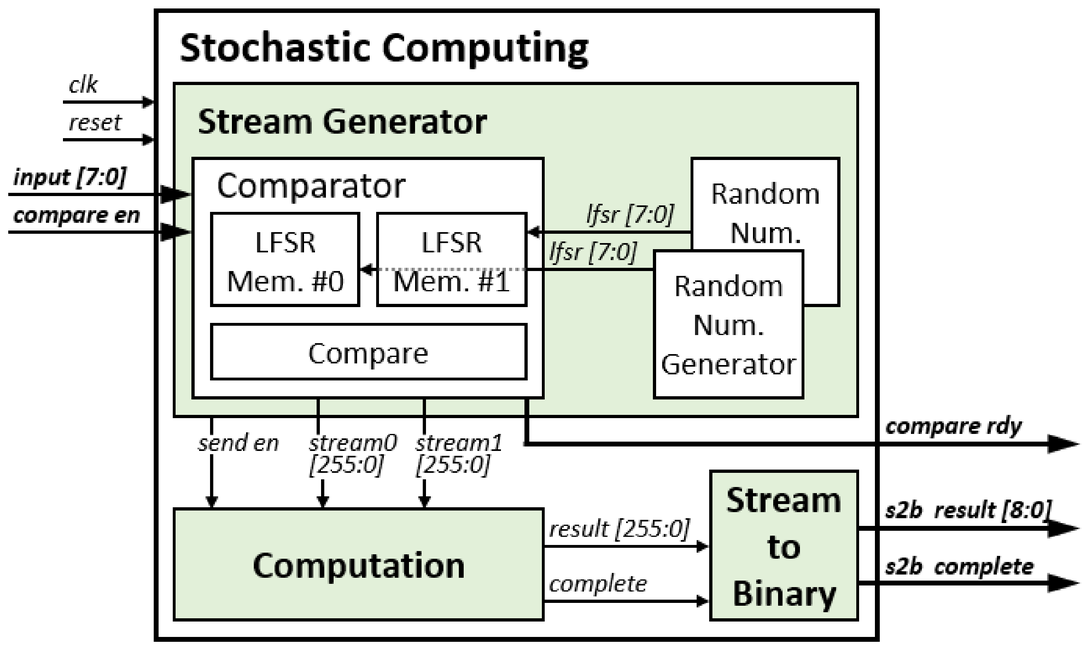
In this paper, we propose a stochastic computing that replaces a multiplication with a logic operation. The stochastic computing enables embedded systems to apply the AI technology. We fabricates the stochastic computing based a machine learning system.

System Architecture

We designed a machine learning system with based on k-nearest neighbor (k-NN) and radial basis function (RBF) algorithm to verify our stochastic computing design. Neuron cell (N-cell) modules of the machine learning system operate calculation for k-NN and RBF. The stochastic computing module multiplication in the neuron cell module. The random number generator of the stochastic computing has the initial value to operate XOR operation. The input data convert to two stochastic streams in the stream generator using the random number. After that, the data is multiplied with two stream data by the logical AND operation. The result of computation is converted to the real value of the result by the decoder.



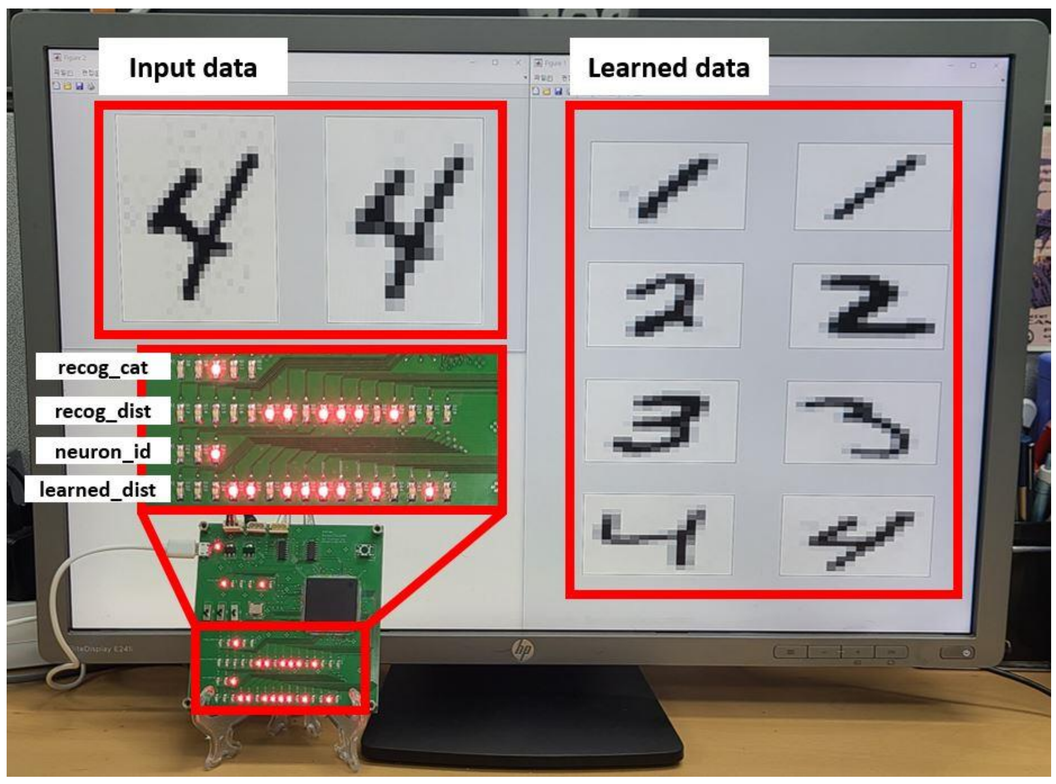
[The Architecture of the Entire System]



[The Architecture of Stochastic Computing]

Chip Verification

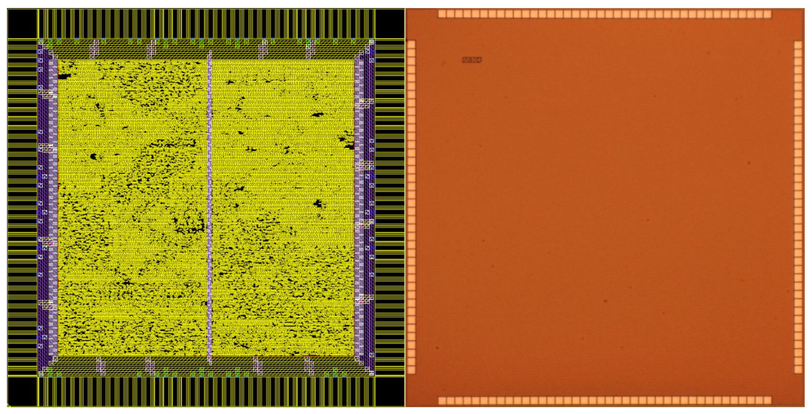
The experimental environment consists of the host PC to transfer the dataset, the prototype PCB including the STJSY and the serial port. The processor performs the learning/recognition operation based on the pre-processed data through the host PC. After that, the result is shown on the led of PCB.



[Experimental environment]

Chip Implementation

Chip specification	
Technology	180nm CMOS
Power Supply	3.3V
Core Size	3.4mm x 3.4mm
Operating Frequency	50MHz



[The chip photograph of the STJSY]

Conclusion

The proposed design classified the various dataset with algorithms of machine learning. In order to reduce the complex of the multiplication, we apply the stochastic computing to the entire system. The prototype PCB was designed to verify our chip design and we demonstrated the operation of out chip successfully.

Acknowledgment

The chip fabrication and EDA tool were supported by the IC Design Education Center (IDEC), Korea.